P P SAVANI UNIVERSITY

Forth Semester of B. Tech. Examination
May 2019
SECE2040 Computer Organization

20.05.2019, Monday   Time: 09:00 a.m. To 11:30 a.m.   Maximum Marks: 60

Instructions:
1. The question paper comprises of two sections.
2. Section I and II must be attempted in separate answer sheets.
3. Make suitable assumptions and draw neat figures wherever required.
4. Use of scientific calculator is allowed.

SECTION – I

Q - 1	Answer the following. (Any Five)	[05]
(i)	Convert 100101 binary number in to gray code.	
(ii)	CMA is _____ type of instruction.	
(iii)	Define : micro operation	
(iv)	Effective address= _____ + _____	
(v)	Define: Interrupt	
(vi)	_____ table is generated at the end of first pass of an assembler.	
Q - 2 (a)	Draw block diagram of Control unit of basic computer and explain it.	[05]
Q - 2 (b)	Write assembly language program to Add two Double-Precision Numbers.	[05]

OR

Q - 2 (a)	What is instruction cycle? Draw Flowchart for Instruction cycle and explain it	[05]
Q - 2 (b)	Write assembly language program to Subtract two numbers.	[05]
Q - 3 (a)	Assume A = (+8) and B = (+5). Multiply these two numbers using Booth algorithm. Show the step-by-step multiplication process.	[05]
Q - 3 (b)	Write a program to evaluate the following arithmetic statement	[05]

X= [A * (B + C) –D] / (E + F -G)

(i) using a general register computer with three-address instructions,

(ii) using an accumulator type computer with one-address instructions,

(iii) Using a stack organized computer with zero-address operation instructions.

OR

Q - (a)	Show the contents of registers E, A, Q and SC during the process of division of following binary numbers. (Use dividend of eight bits).	[05]

a. 10100011 by 1011

b. 00001111 by 0011

Q - 3 (b)	What is meant by addressing modes? How addressing mode is significant for referring memory? List and explain types of addressing modes with example.	[05]
Q - 4	Attempt any one.	[05]
(i)	What is Interrupt? List and explain types of interrupt.	
(ii)	Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory?	

SECTION – II

Q - 1	Answer the following. (Any Five)	[05]
(i)	What is bubble inside pipeline?	
(ii)	Define: Associative Memory	
(iii)	Define: Interface	
(iv)	Determine the number of clock cycles that processor takes to process 200 tasks in a six-	

(v)	Define: Locality of reference	
(vi)	_____ is used to manage the transfer directly between the IO device and memory.	
Q - 2 (a)	What is cache memory? Explain the organization of cache using Direct mapping.	[05]
Q - 2 (b)	Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.	[05]

OR

Q - 2 (a)	What is content addressable memory (CAM)? Show the hardware organization for the associative memory.	[05]
Q - 2 (b)	What are the different types of hazards (conflicts) that can be found in pipeline processing? What are the possible solutions for resolving each hazard?	[05]
Q - 3 (a)	An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in the address space and memory space? If a page consist of 2K words, how many pages and blocks are there in the system?	[05]
Q - 3 (b)	Differentiate between source initiated and destination initiated strobe method for data transfer.	[05]

OR

Q - 3 (a)	What are the sub-operations that are performed in the four segments pipeline of floating point addition and subtraction? Draw flow chart to explain addition of floating numbers using pipeline.	[05]
Q - 3 (b)	Differentiate between memory mapped I/O and isolated I/O?	[05]
Q - 4	Attempt any one.	[05]
(i)	What is DMA? With the supporting diagram, explain the functionality of DMA controller with the use of all registers and control logics.	
(ii)	Differentiate between loosely coupled and tightly coupled multiprocessor system in terms of memory.	

****